

Amendments to the Claims

1. (CURRENTLY AMENDED) An active matrix array, comprising:
an array of matrix elements ~~(10)~~ arranged in rows and columns, each matrix element ~~(10)~~ comprising a circuit;
a plurality of column conductors ~~(16)~~, each arranged for inputting data signals to, or outputting data signals from, the matrix elements ~~(10)~~ of a respective column in first time periods ~~(140)~~; and
means for providing power supply voltages ~~(V1, V2)~~ for the circuit to the matrix element ~~(10)~~ via the column conductors ~~(16)~~ in first time periods ~~(130)~~ interspersed between the first time periods ~~(140)~~.

2. (CURRENTLY AMENDED) An active matrix array according to claim 1, wherein the means for providing power supply voltages ~~(V1, V2)~~ for the circuit to the matrix element ~~(10)~~ via the column conductors ~~(16)~~ comprises, in each matrix element ~~(10)~~, differentiating means for operating differently according to whether the column conductors ~~(16)~~ are being supplied with the power supply voltages ~~(V1, V2)~~ or whether the column conductors ~~(16)~~ are being supplied with the data signals.

3. (CURRENTLY AMENDED) An active matrix array according to ~~claim 1 or 2,~~ claim 1, wherein the array further comprises means ~~(32)~~ for receiving a control signal to the matrix elements ~~(10)~~, the control signal being such as to indicate to the matrix elements ~~(10)~~ when the column conductors ~~(16)~~ are being supplied with the power supply voltages ~~(V1, V2)~~ and when the column conductors ~~(16)~~ are being supplied with the data signals; and wherein the differentiating means in each matrix element ~~(10)~~ comprise means for operating differently in response to the control signal.

4. (CURRENTLY AMENDED) An active matrix array according to ~~any of claims 1 to 3,~~ claim 1, wherein the matrix elements ~~(10)~~ are pixels for a display device; and each pixel comprises, in addition to a respective one of the circuits, a

pixel electrode (18) and a pixel select switching means (12) coupled to the pixel electrode (18).

5. (CURRENTLY AMENDED) An active matrix array according to claim 4, wherein the circuit is a refresh circuit for refreshing the pixel electrode (18).

6. (CURRENTLY AMENDED) An active matrix array according to ~~claim 5 when dependent from claim 3~~ claim 3, wherein the pixels are adapted such that the control signal is used to indicate to the pixel when the column conductors (16) are carrying the power supply voltages (V1, V2) and to switch the pixel from a state where the pixel electrode (18) receives picture data from the column conductors (16) to a state where the pixel electrode (18) receives inverted refresh picture data from the refresh circuit.

7. (CURRENTLY AMENDED) An active matrix array according to ~~any of claims 1 to 6~~ claim 1, wherein the circuit comprises a CMOS inverter (70).

8. (CURRENTLY AMENDED) An active matrix array of ~~any of claims 3 to 7~~ claim 3 wherein the means (32) for receiving a control signal is coupled to the gate of a first control thin film transistor, TFT (52), arranged to allow picture data to be provided to the pixel electrode (18) only when the control signal is set such as to turn the first control TFT (52) on.

9. (CURRENTLY AMENDED) An active matrix array according to claim 8, wherein the means (32) for receiving a control signal is coupled to the gate of a second control TFT (53) arranged to allow refresh data to be provided from the refresh circuit to the pixel electrode (18) only when the control signal is set such as to turn the second control TFT (53) on and the first control TFT (52) off.

10. (CURRENTLY AMENDED) An active matrix array according to claim 9, wherein the means (32) for receiving a control signal is coupled to the gate of a third control TFT (57) arranged to allow the power supply voltages (V1, V2) to be

supplied to the refresh circuit only when the control signal is set such as to turn the second and third control TFTs (~~53, 57~~) on and the first control TFT (~~52~~) off.

11. (CURRENTLY AMENDED) An active matrix array according to ~~any of claims 1 to 10~~ claim 1, wherein a first power supply voltage level (~~V1~~) is supplied to the circuits of a first column of matrix elements (~~10~~) via a first column conductor (~~16a~~) arranged to also input or output data signals to or from the first column of matrix elements (~~10~~), and a second power supply voltage level (~~V2~~) is supplied to the circuits of the first column of matrix elements (~~10~~) via a second column conductor (~~16b~~) arranged to also input or output data signals to or from a second column of matrix elements (~~10~~).

12. (CURRENTLY AMENDED) A method of operating an active matrix array device comprising an array of matrix elements (~~10~~) arranged in rows and columns, wherein each matrix element (~~10~~) comprises a circuit requiring power supply voltages (~~V1, V2~~) to be supplied to the circuit, the method comprising:

in first time periods (~~140~~), inputting a data signal to, or outputting a data signal from, the matrix element (~~10~~) via column conductors (~~16~~); and

in first time periods (~~130~~) interspersed with the first time periods (~~140~~), providing the power supply voltages (~~V1, V2~~) to the circuit via the column conductors (~~16~~).